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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/686,243	10/14/2003	Vikram Kowshik	ATM-279	7611

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EXAMINER	
THAI, TUAN V	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/686,243	KOWSHIK ET AL.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/20/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 5, 8 and 11* is/are rejected.

7)☒ Claim(s) *2-4, 6-7, 9-10 and 12-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/14/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. This action is responsive to IDS filed on January 20, 2004. Claims 1-13 are presented for examination.

2. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 11 are rejected under 35 U.S.C. § 102(b) as being anticipated by Kozaru et al. (USPN: 5,991,223); hereinafter Kozaru.

As per claim 1; Kozaru teaches the invention as claimed including a method of synchronous reading for a plurality of words in a memory system (e.g. see abstract; column 9, lines 38 et seq.) comprises selecting said plurality of words to be read (e.g. see column 13, lines 64-65), the plurality of words having

a first group of words and at least one subsequent group of words; for example, memory array 1 contains multiple group of sub-arrays MA#0-MA#3 having multiple group of words (e.g. see column 13, lines 32 et seq.); reading said plurality of words into a plurality of data registers during a clock latency period (e.g. see column 14, lines 21 et seq.); and shifting out said plurality of words synchronously at the end of said latency period (e.g. see column 61-65).

As per claim 11, Kozaru discloses a burst mode operation system for fast synchronous reading in a memory system (e.g. see abstract) comprises a burst controller is taught a control circuit 902 for controlling burst operation adapted to receive an input clock signal, a variable latency signal, and a burst sequence control signal from said memory system to produce a plurality of words to be read and an output clock signal (e.g. see figure 27, column 1, lines 32 et seq.); an address controller is taught as read/write address circuit 910 coupled to said burst controller for producing addresses of said plurality of words to be read (e.g. see column 2, lines 6 et seq.); a two-tier column decoder is taught as column decoder 908c (e.g. see figure 29) adapted to receive said addresses from said address controller for producing a first tier address and a second tier address (e.g. see column 3, lines 53 et seq.); and a row decoder is taught as global row decoder 908b (e.g. see figure 29) adapted to receive said addresses from said address controller for producing

row addresses of said plurality of words to be read (e.g. see column 3, lines 50 et seq.).

Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozaru et al. (USPN: 5,991,223); hereinafter Kozaru, in view of Khang et al. (USPN: 6,111,808), hereinafter Khang.

As per claims 5 and 8, Kozaru discloses a two-tier column decoder to facilitate synchronous reading of a plurality of words in a synchronous memory system 1 (e.g. see figure 5; column 3, lines 46 et seq.) comprises a sub bitline decoder is equivalently taught as global row decoder 5a coupled to a main bit line of said memory system for decoding row address signal from the address register (e.g. see figure 5; column 13, lines 38 et seq.); a first tier decoder is equivalently taught as decoder 5b coupled to global row decoder 5a to select both said even and odd addresses of said plurality of words for a first

reading during a clock latency period (e.g. see figure 5; column 13, lines 40 et seq., lines 65 bridging column 4, line 9); and a second tier decoder is taught as block decoder 4 coupled to first tier decoder 5b to select either said lower or higher word addresses for a subsequent reading (e.g. see figure 5; column 14, lines 28 et seq.). Kozaru discloses the invention as claimed; Kozaru however does not particularly teach the global row decoder 5a for decoding a most significant bit of said plurality of words to be read and for determining whether an address of said plurality of words is in an low or high order word. Khang discloses the missing element that is known to be required in the system of Kozaru in order to arrive at the Applicant's current invention wherein Khang discloses the row decoder for decoding the a sub word line enable selection signal (SWLE) and a global word line signal (GWLb) utilized the most significant bit (MSB) and least significant bit address (LSB) scheme for determining locations of the address data/word (e.g. see abstract; column 4, lines 55 et seq.). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention as made to employ the teaching of Khang wherein MSB and LSB addressing decoding scheme is utilized for determine address data/word location for that of Kozaru system. In doing so, first of all, it would allow location of the word address to be quickly recognized thru the implementation of least and most significant bit address;

secondly, the system throughput would be greatly enhanced since decoding the MSB would take less number of system clock cycles, therefore being advantageous.

As per claim 8, see arguments with respect to claim 5. It encompasses the same scope of invention as to that of claim 5, the claim is therefore rejected for the same reasons as being set forth above.

Allowable subject matter

7. Claims 2, 6, 9, 12 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and intervening claims. Claims 3-4, 7 and 10 are also allowable since it is depended upon the indicated allowable claims 2, 6 and 9 respectively.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see ***http://pair-direct.uspto.gov***. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/October 12, 2005

Tuan V. Thai
PRIMARY EXAMINER
Group 2100